

Goldgeisser et al
Application No.: 09/993,191
Attorney Docket No. 005-1
Page 5

REMARKS

Claims 6 and 7 have been examined and claims 6 and 7 are amended and are pending in the application. It is noted with appreciation that claims 6 and 7 are deemed to be directed toward allowable subject matter. Reexamination and reconsideration of all outstanding objections and
5 rejections is requested.

Claims 6 and 7 have been amended to clarify the roles of the input signals in defining the ternary logic states which can be latched by embodiments of the invention defined by those claims.

As described in the specification at paragraphs [7] and [8], page 2, lines 12-15, the
10 circuit of Fig. 1 possesses two stable operating points and the latch can be programmed by injecting differential impulse currents to force the latch to a desired operating point. Further paragraph [45], page 5, lines 15-18, describes that in the stable states of an embodiment of a bistable latch one transistor is biased full ON and the other transistor is OFF.

The manner in which the input signals define the ternary states is described in
15 paragraph [59] for the embodiment depicted in Fig. 13. The first and second bistable ternary states are latched when voltage levels of inp and inn differ by a specified voltage level and the third stable ternary state is latched when the signal levels are equal.

Fig. 13(b) depicts the general formation of a latch utilizing any of the tri-stable circuits described in the application. Figures in the form of Figures 9-12 are used by persons of skill
20 in the art when designing latch circuits and the specific signal inputs are not depicted in the diagrams. However, input structures, such as depicted in Figs. 13 and 13(a), are well-known in the art and are utilized to form a latch from any of the circuits schematically depicted in Figs. 9-12.

CONCLUSION

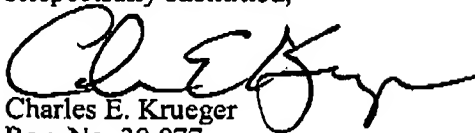
25 In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 944-3320.

Goldgeisser et al
Application No.: 09/993,191
Page 6

PATENT

Respectfully submitted,



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10